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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,233	03/27/2001	Ryo Kubota	Q62494	8072

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,233	KUBOTA ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 16, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (US 6,194,758).

In re claim 1, Tanaka et al. teach the claimed method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit (i.e. a peripheral circuit region) and a DRAM (i.e. a memory cell region) on a same semiconductor chip 1, comprising:

- providing a CMOS logic circuit portion and a DRAM portion on a substrate 1 (Fig.18);
- forming a first transistor 42c/43c on the substrate 1 at the CMOS logic circuit portion (Fig. 18);
- forming a second transistor 42b/43b on a substrate 1 at the DRAM portion (Fig. 18);
- forming an interlayer film 59/60 on the substrate 1 at the CMOS logic circuit portion and on the substrate 1 at the DRAM portions, covering the first transistor 42c/43c and the second transistor 42b/43b (Fig.18);
- forming a groove 61 in the interlayer film 59/60 by removing a portion of the interlayer film 59/60 at the DRAM portion (Fig.18);

- forming a first polysilicon film 62 on an upper surface of the interlayer film 59/60 at the CMOS logic circuit portion and at the DRAM portions, and a second polysilicon film 62 on an inner wall of the groove 61 at the DRAM portion (Fig.18);
- forming a first HSG 74 on a surface of the first polysilicon film 62 at the CMOS logic portion and a second HSG 74 on a surface of the second polysilicon film 62 at the DRAM portion (Fig.18);
- removing the first HSG 74 and the first polysilicon film 62 from the CMOS logic circuit portion (i.e. the peripheral circuit region) by a CMP process to expose the top surface of the interlayer film 59/60 and retaining at least a portion of the HSG 74 in the groove 61 (from Fig. 18 to Fig.19);
- forming a capacitor dielectric film 150 on the second HSG film 74 in the groove 61 and on the exposed surface of the interlayer film (from Fig.20 to Fig.21); and
- forming an upper electrode 151 on the capacitor dielectric film 150 (Fig.21).

In re claim 16, Tanaka et al. teach the claimed method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit (i.e. a peripheral circuit region) and a DRAM (i.e. a memory cell region) on a same semiconductor chip 1, comprising:

- providing a CMOS logic circuit portion and a DRAM portion on a substrate 1 (Fig.18);
- forming a first transistor 42c/43c on the substrate 1 at the CMOS logic circuit portion (Fig. 18);
- forming a second transistor 42b/43b on a substrate 1 at the DRAM portion (Fig. 18);

- forming an interlayer film 59/60 on the substrate 1 at the CMOS logic circuit portion and on the substrate 1 at the DRAM portions, covering the first transistor 42c/43c and the second transistor 42b/43b (Fig.18);
- forming a groove 61 in the interlayer film 59/60 by removing a portion of the interlayer film 59/60 at the DRAM portion (Fig.18);
- forming a polysilicon film 62 on said interlayer film 59/60 at said CMOS logic circuit portion and at said DRAM portions, and on an inner wall of said groove 61 at said DRAM portion (Fig.18);
- forming an HSG 74 on a surface of said polysilicon film 62 (Fig.18);
- removing said HSG 74 and said polysilicon film 62 from an upper surface of said of said interlayer film 59/60 from said CMOS logic circuit portion (i.e. the peripheral circuit region) retaining at least a portion of said HSG 74 in said groove 61 and at least a portion of said polysilicon 62 in said groove 61 (from Fig. 18 to Fig.19);
- forming a capacitor dielectric film 150 on said portion of said HSG film 74 in said groove 61 and on said exposed surface of the interlayer film after removing said HSG 74 and said polysilicon film 62 (from Fig.20 to Fig.21).

In re claim 22, Tanaka et al. also teach that the step of removing first HSG 74 and the first polysilicon 62 comprises a step of exposing a part of the interlayer film 59/60 (from Fig.18 to Fig.19); the step of forming said capacitor dielectric film 150 comprises a step of forming a first capacitor dielectric film 150 on said part of said interlayer film 77 (which is equivalent to 59) and a second capacitor dielectric film 150 on said second HSG 74 within the groove 61 (Fig. 21) after removing said first HSG 74 and said first polysilicon film 62;

and the step of forming an upper electrode 151 comprising forming an upper electrode 151 on said first capacitor dielectric film 150 (i.e. the 150 formed on the surface of 77) and said second capacitor dielectric film 150 (i.e. the 150 formed within the groove 61).

In re claim 23, Tanaka et al. teach a method of manufacturing a semiconductor device comprising:

- forming a transistor 42b/43b on a substrate 1 (Fig. 18);
- forming an interlayer film 59/60 on the substrate 1 to cover the transistor 42b/43b (Fig. 18);
- forming a groove 61 in the interlayer film 59/60 (Fig.18);
- forming a first polysilicon film 62 on an upper surface of the interlayer film 59/60 and a second polysilicon film 62 on an inner wall of the groove 61 (Fig. 18);
- forming a first HSG 74 on a surface of the first polysilicon film 62 and a second HSG 74 on a surface of the second polysilicon film 62 (Fig.18);
- removing the first HSG 74 and the first polysilicon film 62 to expose a part of the interlayer film 59/60 while leaving the second HSG 74 in the groove 61 (from Fig.18 to Fig.19);
- forming a capacitor dielectric film 150 on the second HSG film 74 in the groove 61 and on said part of the interlayer film 77 (Fig. 21); and
- forming an upper electrode 151 on the capacitor dielectric film 150, said upper electrode 151 free from contacting said interlayer film 77 (Fig.21).

3. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Tu (US 6,200,898).

Tu teaches a method of manufacturing a semiconductor device comprising:

- forming a transistor 2/3/4/6 on a substrate 1 (Fig. 1);
- forming an interlayer film 7/10/13/14 on the substrate 1 to cover the transistor 2/3/4/6 (Fig. 2);
- forming a groove 16 in the interlayer film 7/10/13/14 (Fig.3);
- forming a first polysilicon film 17a on an upper surface of the interlayer film 7/10/13/14 and a second polysilicon film 17a on an inner wall of the groove 16 (Fig. 4);
- forming a first HSG 18 on a surface of the first polysilicon film 17a and a second HSG 18 on a surface of the second polysilicon film 17a (Fig.4);
- removing the first HSG 18 and the first polysilicon film 17a to expose a part of the interlayer film 7/10/13/14 while leaving the second HSG 18 in the groove 16 (from Fig.4 to Fig.5);
- forming a capacitor dielectric film 22 on the second HSG film 18 in the groove 16 and on said part of the interlayer film 7/10/13/14 (Fig. 8); and
- forming an upper electrode 23 on the capacitor dielectric film 22, said upper electrode 23 free from contacting said interlayer film 7/10/13/14 (Fig.9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 3 and 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US '758) in view of Sung (US 5,858,831).

In re claims 2 and 17, Tanaka et al. teach forming a first gate insulating layer 42c in the first transistor 42c/43c and forming a second insulating layer 42b in the second transistor 42b/43b but do not teach that the first insulating layer 42c is thinner than the second insulating layer 42b.

Sung teaches forming a first insulating layer 7 (thickness: 40~60 Å) in the logic circuit portion 50 and a second gate insulating layer 8 (thickness: 50~70 Å) in the DRAM portion 60 (Fig. 8; col. 4, lines 21-25).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to combine Tanaka et al. with Sung so that the first insulating layer 42c in Tanaka et al. is thinner than the second insulating layer 42b in Tanaka et al., as suggested by Sung (col. 4, lines 21-25), since by doing so it would be beneficial to the dielectric constant adjustment in the first and the second transistors.

In re claim 3, Tanaka et al. teach the second transistor comprises a peripheral circuit transistor 42c/43c and a switching transistor 43d/42d and the peripheral circuit transistor 42c/43c and the switching transistor 43d/42d have similar structure (Fig.18).

In re claims 18, 20 and 21, Tanaka et al is silent as to doping the polysilicon of the gate electrode 43c with born, wherein the first transistor 42c/43c comprise a p-channel transistor.

Sung, however, teaches the polysilicon of the gate electrode 9c is a p-type doping, such as born-doping (Fig.18 and col. 5, lines 13-20), wherein the first transistor 7/9c/16/17/18 comprise a p-channel transistor; and an n-type transistor 7/9b/16/17/18 having a gate electrode 9b which is made of polysilicon doped with phosphorous (Fig.18).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to combine Tanaka et al. with Sung so that a p-channel transistor with born-doped polysilicon and a n-channel transistor with phosphorous-doped polysilicon is formed in the logic circuit portion Tanaka et al., since by doing so it would form a complete logic circuit portion.

6. Claims 4-7, 9, 12-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US '758) in view of Sung, as applied to claims 2, 3, 17, 18, 20 and 21, and further in view of AAPA ("applicant's admitted prior art")

In re claims 4, 12, 13 and 19, Tanaka et al. teach forming an interlayer film 59/60 comprises steps of forming a first interlayer film 59 comprises a silicon oxide layer (col. 18, line 43) and forming a second interlayer film 60 comprising a BSG film (i.e. boron-doped silicon oxide)(col. 18, lines 44-45). Tanaka et al. do not teach that the second interlayer film 60 is a BPSG film. However, BPSG is an art-recognized equivalence to BSG in the application of interlayer film, as evidenced by AAPA.

AAPA teaches utilizing the BPSG as the second interlayer film 120 over the first interlayer film 116 (SiO2; Figs. 3C-3D) in the DRAM portion.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to replace BSG of Tanaka et al. with BPSG of AAPA used as the second interlayer, since BPSG is an art-recognized equivalent dielectric to BSG as the interlayer layer.

In re claims 5-6, Tanaka et al. teach forming an opening 61 in the first interlayer 59 (Fig.11) over a diffusion region 201b of the switching transistor 43b/44b (Fig. 11); forming a capacitor

electrode 62 in the opening 61 in the first interlayer film 59 (Fig.11), wherein the capacitor electrode 62 is connected to the diffusion region 201b of the switching transistor 42b/43b via a plug 57 (Fig. 11); the groove 61 is formed in the second interlayer film 60 (Fig. 11) and the second polysilicon 62 (the portion of 62 formed on the surface of the interlayer layer 60) is connected to the capacitor electrode 62 (i.e. the portion of 62 formed in the opening 61) (Fig. 18).

In re claim 7, Tanaka et al. inherently teach forming a first photoresist layer on the first HSG and a second photoresist layer on the second HSG and removing the first photoresist layer to expose the first HSG (i.e. the HSG formed in the opening 61) (from Fig.18 to Fig.19 and col. 20, lines 41-45).

In re claim 9, Tanaka et al. do not expressly teach the capacitor dielectric film 150 comprising Ta2O5 but do suggest that the capacitor dielectric film 150 can be an insulator with a high dielectric constant (col. 19, lines 8-9).

AAPA teaches utilizing a high-dielectric-constant material such as Ta2O5 for capacitor dielectric film in DRAM application (page 2, lines 12-13).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to utilize the high-dielectric-constant material such as Ta2O5, as suggested by AAPA, for capacitor dielectric film in the method of Tanaka et al., since by doing so it would improve the performance of the capacitor.

In re claims 14 and 15, the selection of the surface area ratio of the memory cell portion is obvious because it is a matter of determining optimum process condition by routine experimentation for best results for the DRAM performance in conjunction with the

consideration the size of CMOS logic circuit portion. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In fact, AAPA teaches that the ration of memory cells 1 to the area of the chip 2 can be 50~60% (Fig. 6A; page 12, lines 14-16). In such situation, the applicants must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05 III

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (7:30 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

August 25, 2005

HSIEN-MING LEE
PRIMARY EXAMINER